What is claimed is:

1. A method for fabricating a bottle-shaped trench capacitor, comprising the steps of:

forming a trench in a substrate;

filling a lower portion of the trench with a first conductive layer surrounded by a doped layer;

forming a conformable insulating layer overlying the substrate and an inner surface of the upper portion of the trench to cover the first conductive layer and the doped layer;

performing a heat treatment on the substrate to form a doping region in the substrate near the doped layer to serve as a buried bottom plate;

anisotropically etching the insulating layer to form a collar insulating layer over a sidewall of an upper portion of the trench;

successively removing the first conductive layer and the doped layer using the collar insulating layer as a mask to expose the surface of the doping region;

etching a portion of the exposed doping region to form a bottle-shaped trench;

successively forming a conformable rugged polysilicon layer and a conformable capacitor dielectric layer in the lower portion of the trench; and

filling the lower portion of the trench with a second conductive layer to serve as a top plate.

2. The method as claimed in claim 1, further successively forming a third conductive layer and a fourth conductive layer overlying the second conductive layer.

3. The method as claimed in claim 2, wherein the third and fourth conductive layers are doped polysilicon layers.

4. The method as claimed in claim 1, wherein the first conductive layer is a polysilicon layer.

5. The method as claimed in claim 1, wherein the doped layer is an arsenic silicate glass (ASG) layer.

6. The method as claimed in claim 5, wherein the doped layer is removed by vapor hydrofluoric (VHF) acid.

7. The method as claimed in claim 1, wherein the insulating layer is tetraethyl orthosilicate (TEOS) oxide.

8. The method as claimed in claim 1, wherein the heat treatment is performed at about 900 to 1100°C.

9. The method as claimed in claim 1, wherein the portion of the exposed doping region is etched by NH_4OH.

10. The method as claimed in claim 1, wherein the second conductive layer is a doped polysilicon.

11. The method as claimed in claim 1, wherein the capacitor dielectric layer comprises a silicon nitride layer.

12. The method as claimed in claim 1, further performing a gas phase doping (GPD) after the rugged polysilicon layer is formed.

13. A method for fabricating a bottle-shaped trench capacitor, comprising the steps of:

providing a substrate covered by a masking layer having an opening therein;

etching the substrate under the opening to form a trench therein;

filling a lower portion of the trench with a polysilicon layer surrounded by a doped silicon oxide layer;

forming a conformable insulating layer overlying the masking layer and an inner surface of the upper portion of the trench to cover the polysilicon layer and the doped silicon oxide layer;

performing a heat treatment on the substrate to form a doping region in the substrate near the doped silicon oxide layer to serve as a buried bottom plate;

anisotropically etching the insulating layer to form a collar insulating layer over a sidewall of an upper portion of the trench;

successively removing the polysilicon layer and the doped silicon oxide layer using the collar insulating layer as a mask to expose the surface of the doping region;

etching a portion of the exposed doping region to form a bottle-shaped trench;

successively forming a conformable rugged polysilicon layer and a conformable capacitor dielectric layer in the lower portion of the trench;

filling the lower portion of the trench with a doped polysilicon layer to serve as a top plate;

successively forming a second doped polysilicon layer and a third doped polysilicon layer overlying the first doped polysilicon layer.

14. The method as claimed in claim 13, wherein the masking layer is composed of a pad oxide layer and an overlying silicon nitride layer.

15. The method as claimed in claim 14, before filling the polysilicon layer, further comprising the steps of:

isotropically etching the pad oxide layer to form a recess with a predetermined depth; and

filling the recess with silicon nitride.

16. The method as claimed in claim 15, wherein the pad oxide layer is etched by buffer hydrofluoric (BHF) acid.

17. The method as claimed in claim 15, wherein the predetermined depth is about 15 to 40Å.

18. The method as claimed in claim 13, wherein the doped silicon oxide layer is an arsenic silicate glass (ASG) layer.

19. The method as claimed in claim 18, wherein the doped silicon oxide layer is removed by vapor hydrofluoric (VHF) acid.

20. The method as claimed in claim 13, wherein the insulating layer is tetraethyl orthosilicate (TEOS) oxide.

21. The method as claimed in claim 13, wherein the heat treatment is performed at about 900 to 1100°C.

22. The method as claimed in claim 13, wherein the portion of the exposed doping region is etched by NH_4OH.

23. The method as claimed in claim 13, wherein the capacitor dielectric layer comprises a silicon nitride layer.

24. The method as claimed in claim 13, further performing a gas phase doping (GPD) after the rugged polysilicon layer is formed.